AMENDMENTS TO THE SPECIFICATION

In the Specification

Please substitute the following amended paragraph(s) and/or section(s) (deleted matter is shown by strikethrough and added matter is shown by underlining):

Page 23, line 8-line 14.

HDLs commonly have constructs that require simulation by the PLI model object code although there is no explicit construct in HDL source, i.e., they are implicit. The most common implicit constructs are implicit wire operations, i.e., logic gates implemented by wire connections (called "wired or" and "wired and"), delay lines (delay logic gates) implemented by trireg wire type in Verilog and continuous assignments implied by instance input and output ports. As shown in block 250, the internal data structures built in block 220, are scanned to locate implicit constructs. The implicit constructs are then analyzed and intermediate code is generated.

Page 5, line 15 through page 6, line 1.

6. PROCEDURAL CONSTRUCTS: Procedural constructs model behavior using parallel HDL "program" execution. Some procedural constructs such as delay controls, always blocks, and fork-join require scheduling. These are called scheduled procedural constructs. Some constructs just compute new values. They are called timing free procedural constructs. Usually a block of timing free procedural code is preceded by and triggered by scheduled procedural code that synchronizes behavioral model execution. HDLs also allow definition of reused groups of statements as tasks or functions. In Verilog, tasks contain both scheduled and timing free procedural constructs. Functions, i.e., function procedural operations, only contain timing free procedural constructs (lines 32-46).